Fig. 1

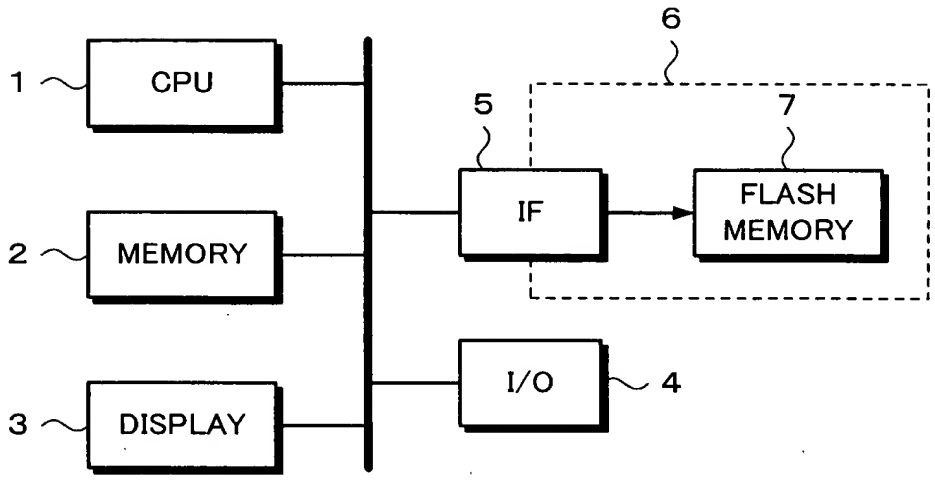

6
1
CPU
5
7
IF
FLASH MEMORY
2
MEMORY
I/O
4
3
DISPLAY

Fig. 2

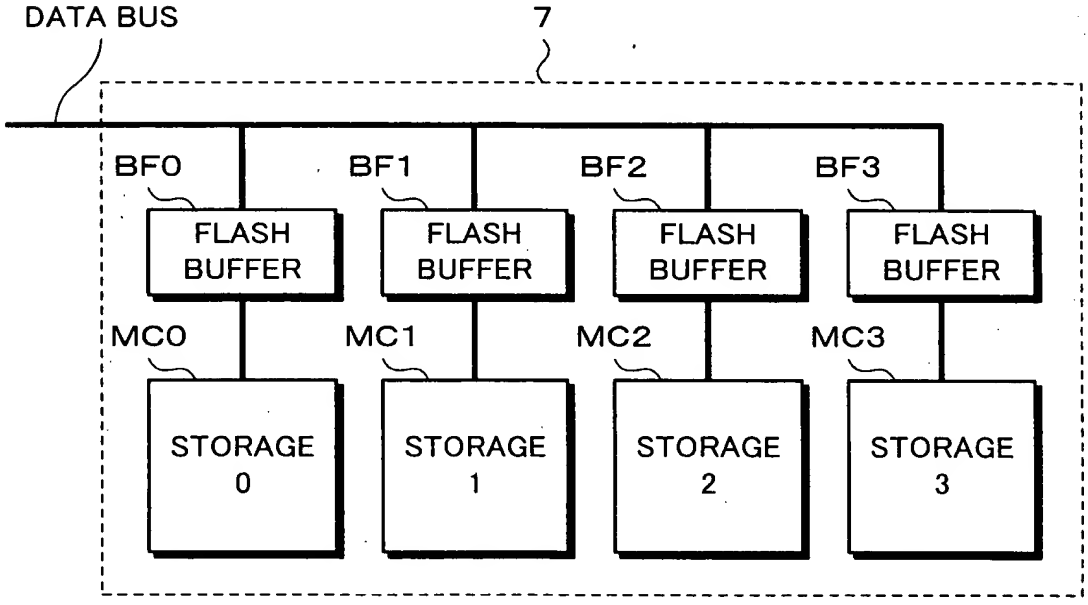

DATA BUS
7
BF0
BF1
BF2
BF3
FLASH BUFFER
FLASH BUFFER
FLASH BUFFER
FLASH BUFFER
MC0
MC1
MC2
MC3
STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3

Fig. 3

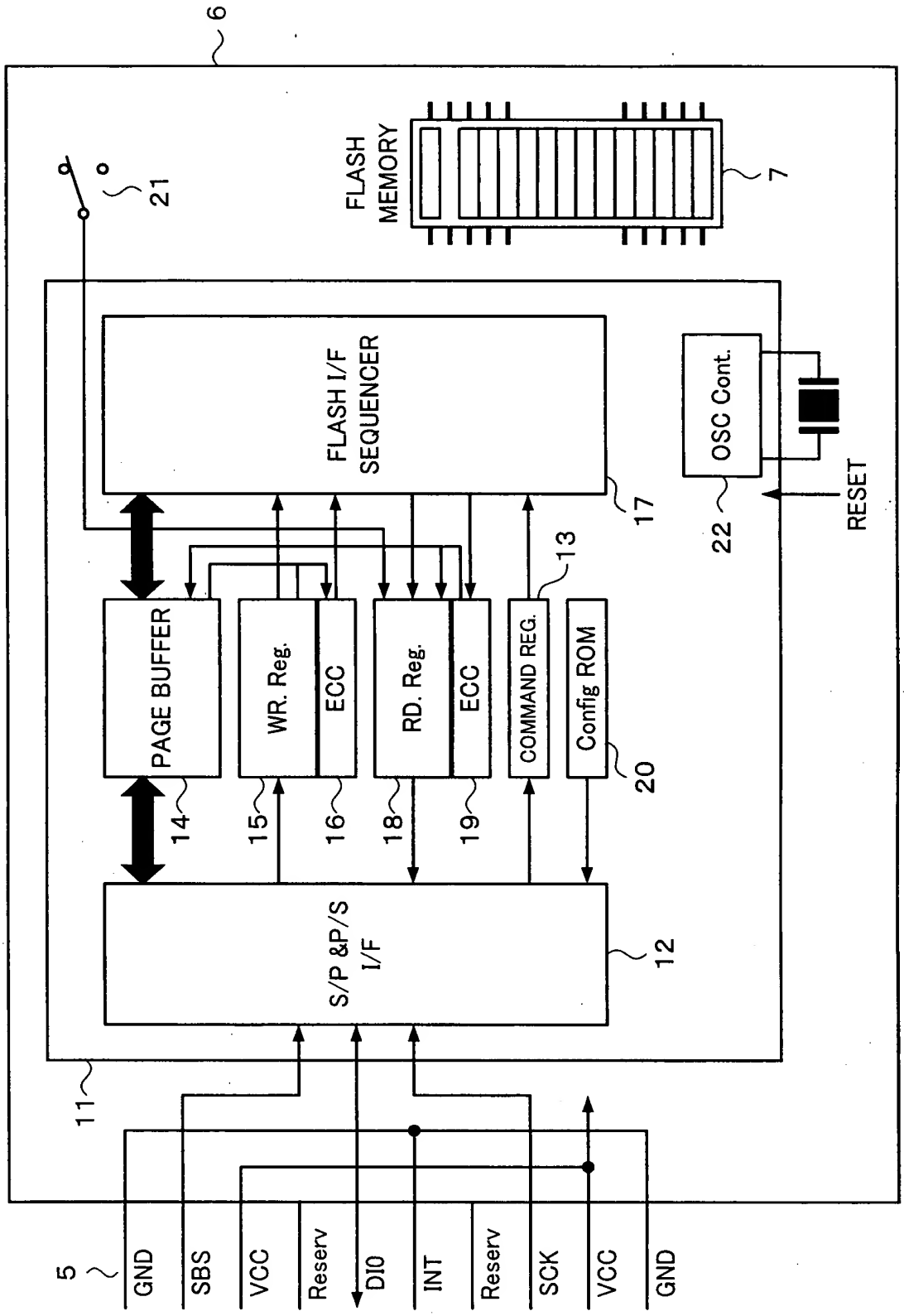

6
21
FLASH MEMORY
7
FLASH I/F SEQUENCER
17
OSC Cont.
22
RESET
13
PAGE BUFFER
14
WR. Reg.
15
ECC
16
RD. Reg.
18
ECC
19
COMMAND REG.
Config ROM
20
S/P &P/S I/F
12
11
5
GND
SBS
VCC
Reserv
DIO
INT
Reserv
SCK
VCC
GND

Fig. 4

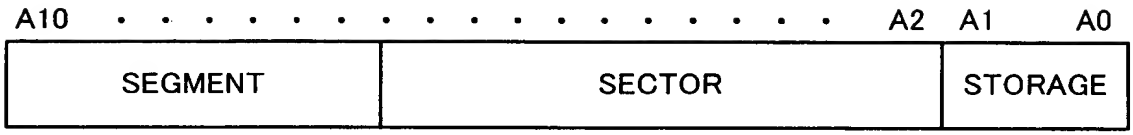

A10
A2
A1
A0
SEGMENT
SECTOR
STORAGE

Fig. 5

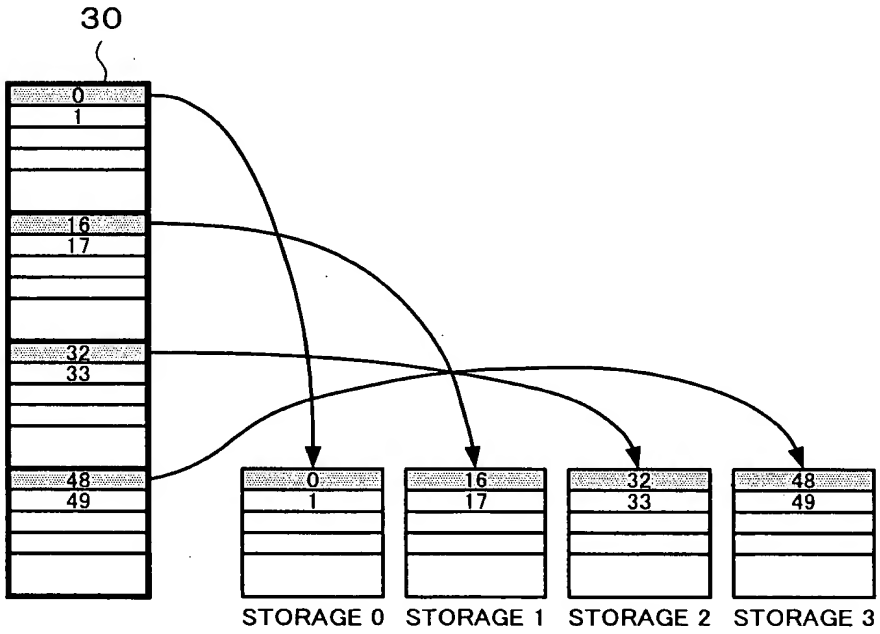

30
0
1
16
17
32
33
48
49
STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3

Fig. 6

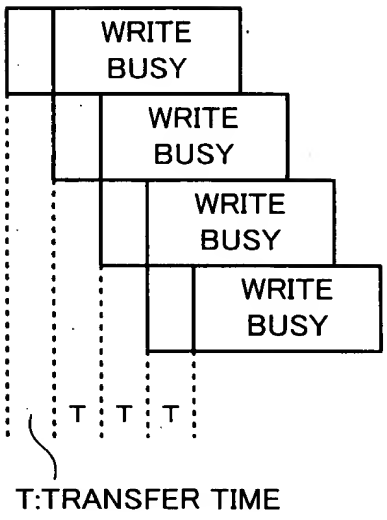

WRITE BUSY
WRITE BUSY
WRITE BUSY
WRITE BUSY
T
T
T
T:TRANSFER TIME

Fig. 7

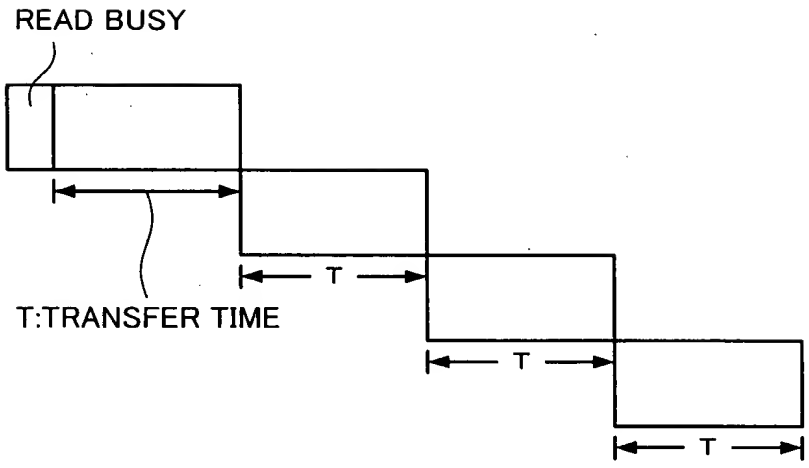

READ BUSY
T
T
T
T:TRANSFER TIME

Fig. 8

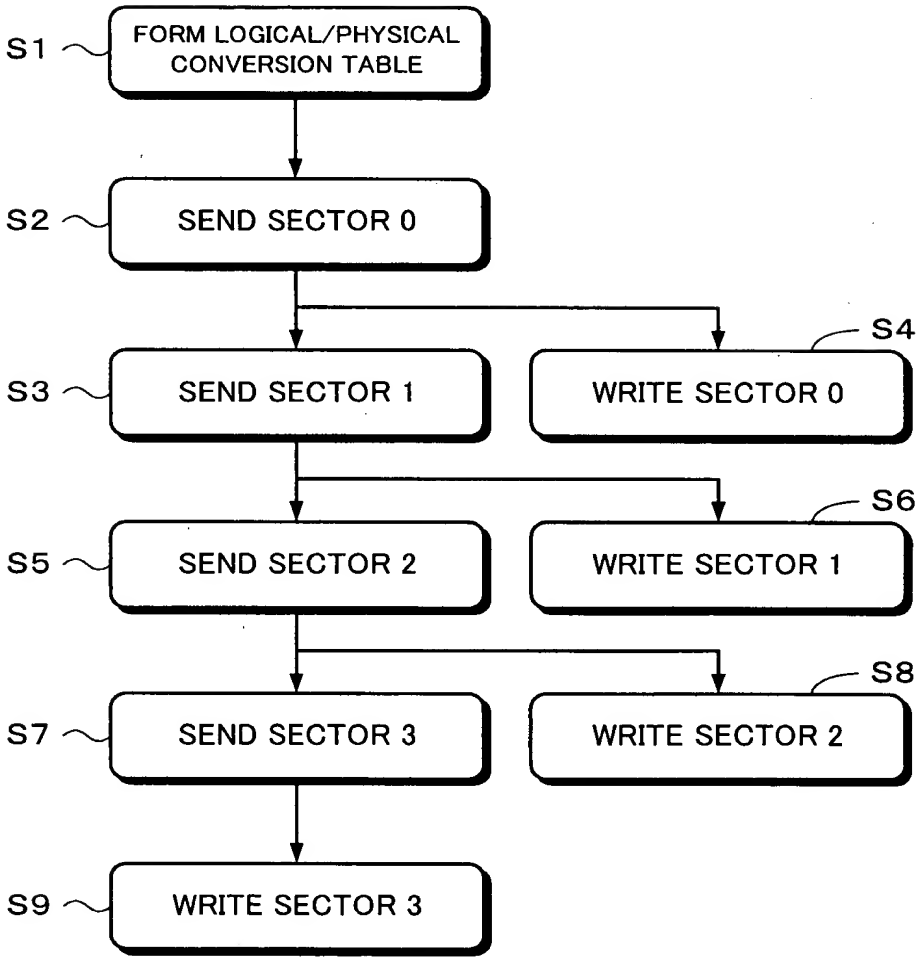

S1
FORM LOGICAL/PHYSICAL CONVERSION TABLE
S2
SEND SECTOR 0
S3
SEND SECTOR 1
S4
WRITE SECTOR 0
S5
SEND SECTOR 2
S6
WRITE SECTOR 1
S7
SEND SECTOR 3
S8
WRITE SECTOR 2
S9
WRITE SECTOR 3

Fig. 9

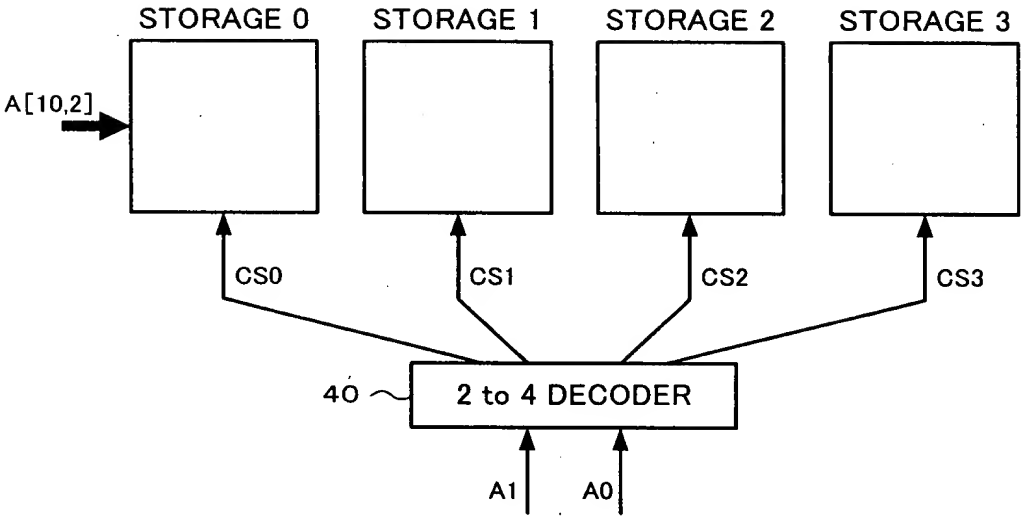

STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3
A[10,2]
CS0
CS1
CS2
CS3
40
2 to 4 DECODER
A1
A0

Fig. 10

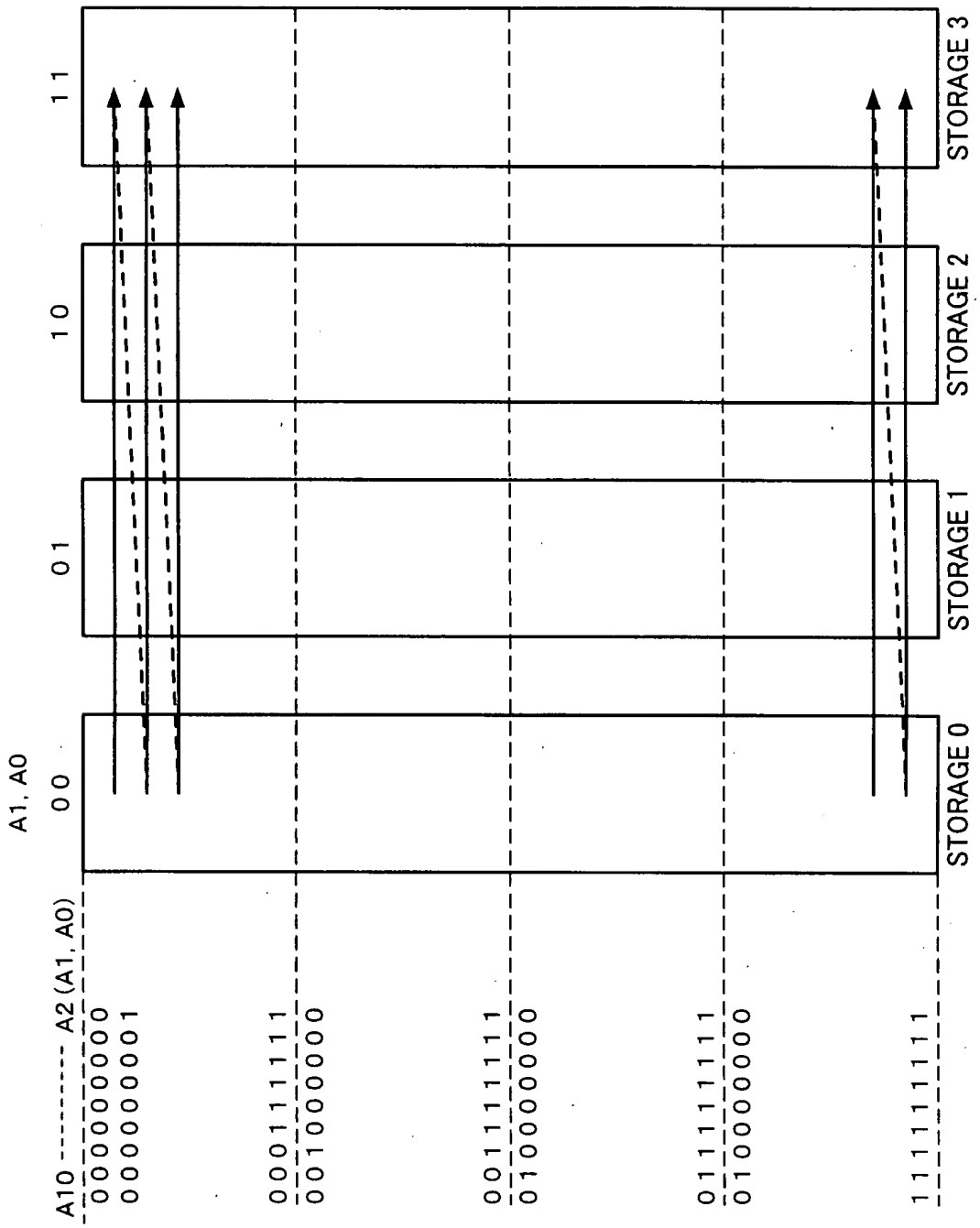

A1, A0
0 0
0 1
1 0
1 1
STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3
A10 ---------- A2 (A1, A0)
0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 1
0 0 0 1 1 1 1 1 1 1
0 0 1 0 0 0 0 0 0 0
0 0 1 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0 0
0 1 1 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1 1 1

Fig. 11

	STORAGE 0	STORAGE 1	STORAGE 2	STORAGE 3
SEGMENT 0	0x0000	0x0001	0x0002	0x0003
	0x0004	0x0005	0x0006	0x0007
	⋮	⋮	⋮	⋮
	0x01fc	0x01fd	0x01fe	0x01ff
SEGMENT 1	0x0200	0x0201	0x0202	0x0203
	⋮	⋮	⋮	⋮
	0x03fc	0x03fd	0x03fe	0x03ff
SEGMENT 2	0x0400	0x0401	0x0402	0x0403
	⋮	⋮	⋮	⋮
	0x04fc	0x04fd	0x04fe	0x04ff
SEGMENT 3	0x0600	0x0601	0x0602	0x0603
	⋮	⋮	⋮	⋮
	0x07fc	0x07fd	0x07fe	0x07ff

Fig. 12

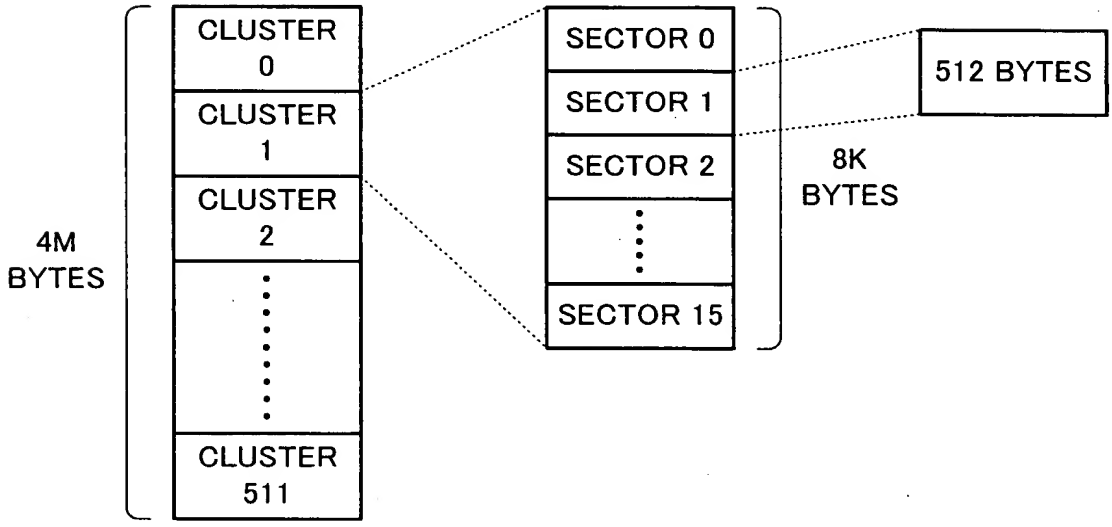


Fig. 13A

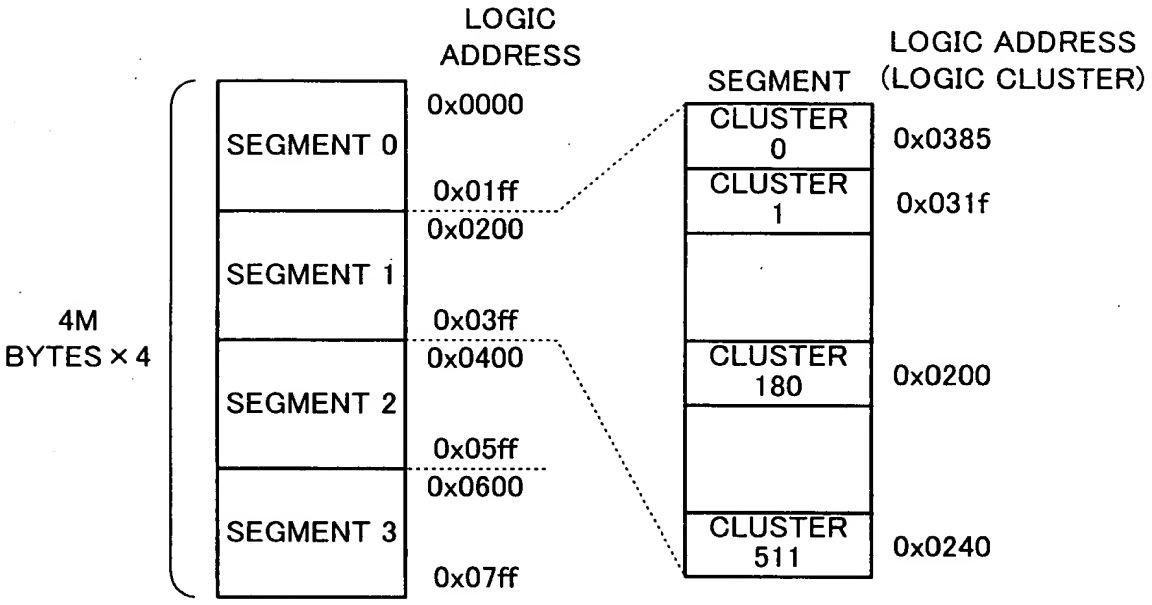


Fig. 13B

LOGIC ADDRESS	PHYSICAL ADDRESS
0x0200	180
0x0240	511
0x031f	1
0x0385	0

Fig. 14

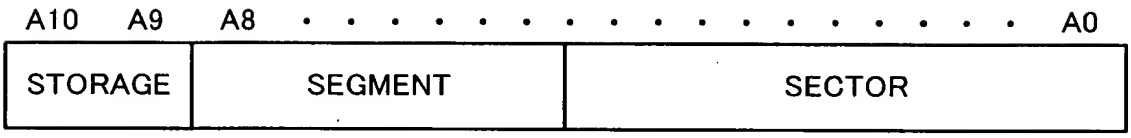


Fig. 15

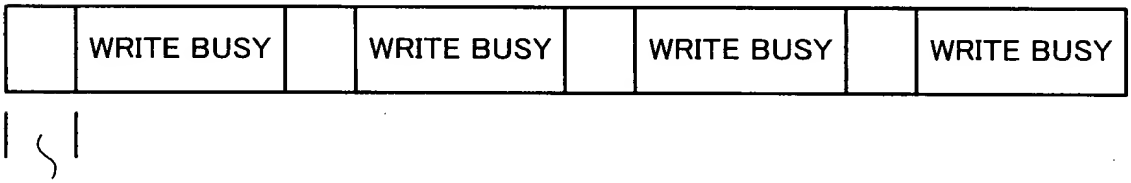


Fig. 16

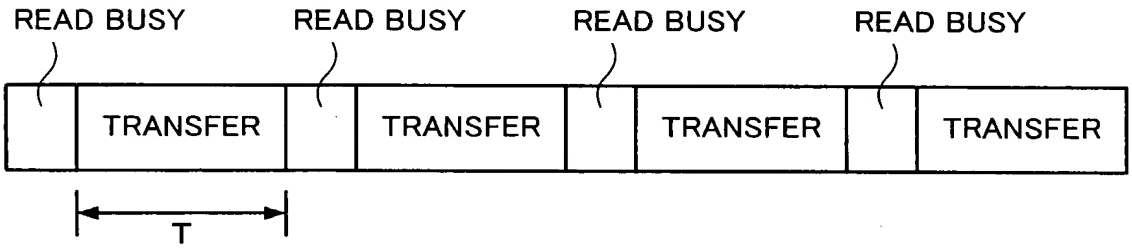


Fig. 17

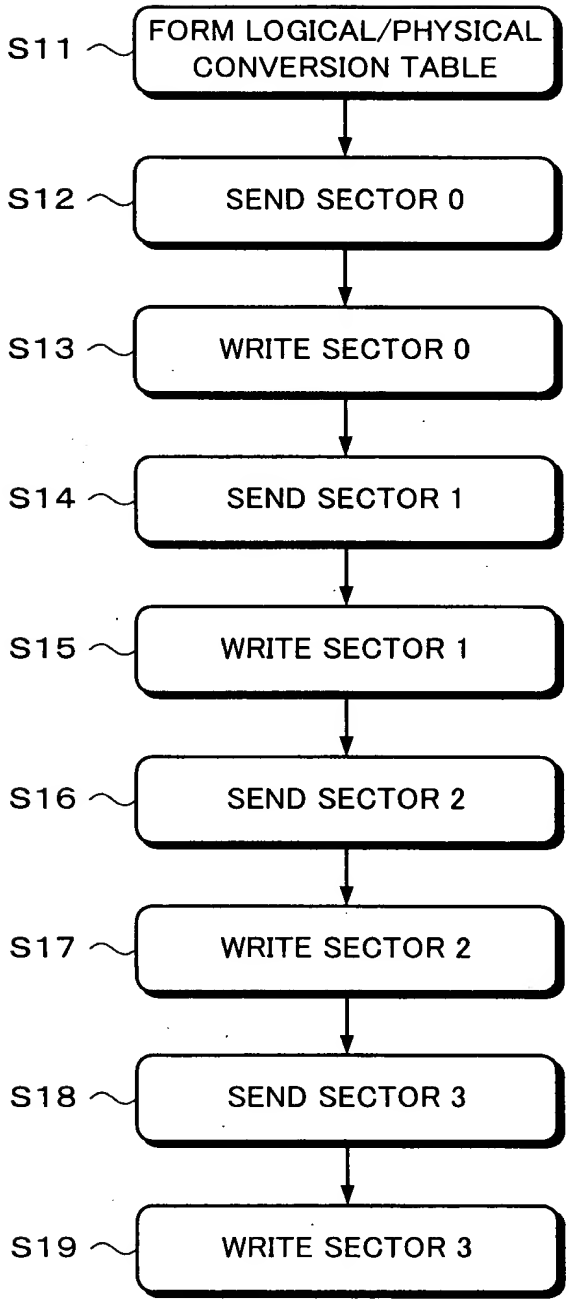

S11
FORM LOGICAL/PHYSICAL CONVERSION TABLE
S12
SEND SECTOR 0
S13
WRITE SECTOR 0
S14
SEND SECTOR 1
S15
WRITE SECTOR 1
S16
SEND SECTOR 2
S17
WRITE SECTOR 2
S18
SEND SECTOR 3
S19
WRITE SECTOR 3

Fig. 18

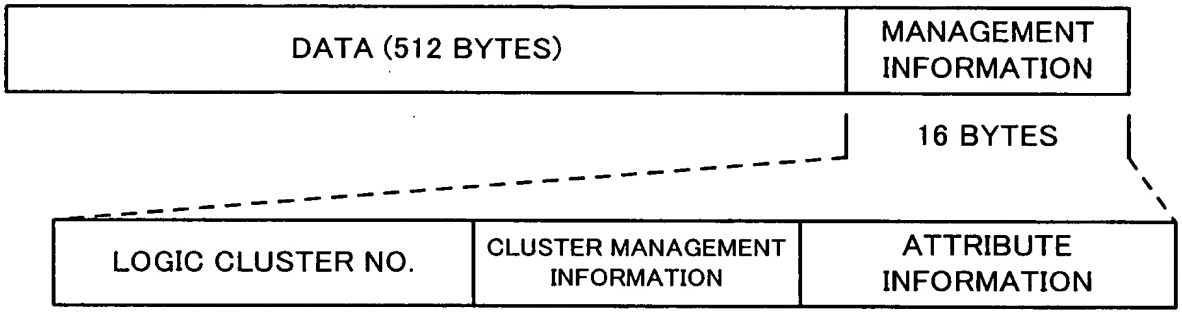

DATA (512 BYTES)
MANAGEMENT INFORMATION
16 BYTES
LOGIC CLUSTER NO.
CLUSTER MANAGEMENT INFORMATION
ATTRIBUTE INFORMATION

Fig. 19

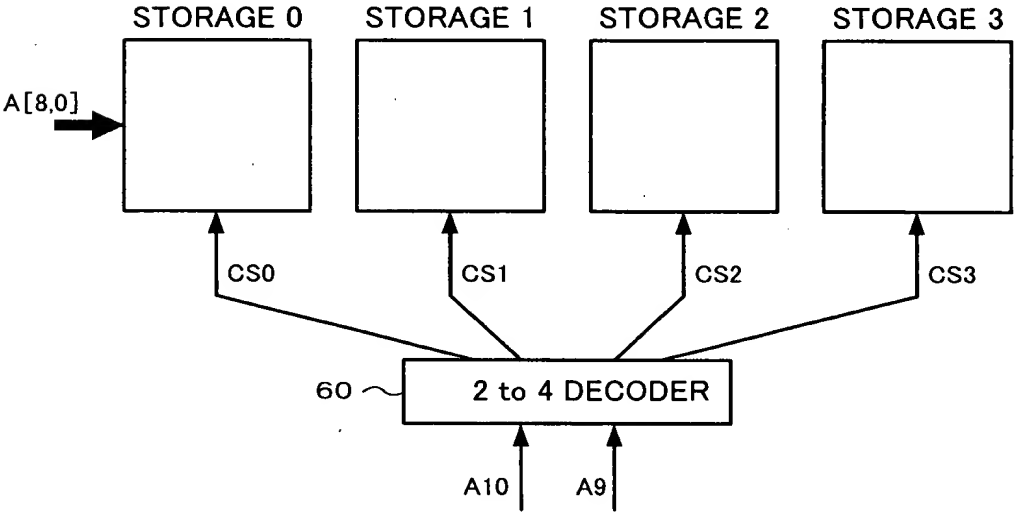

STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3
A[8,0]
CS0
CS1
CS2
CS3
60
2 to 4 DECODER
A10
A9

Fig. 20

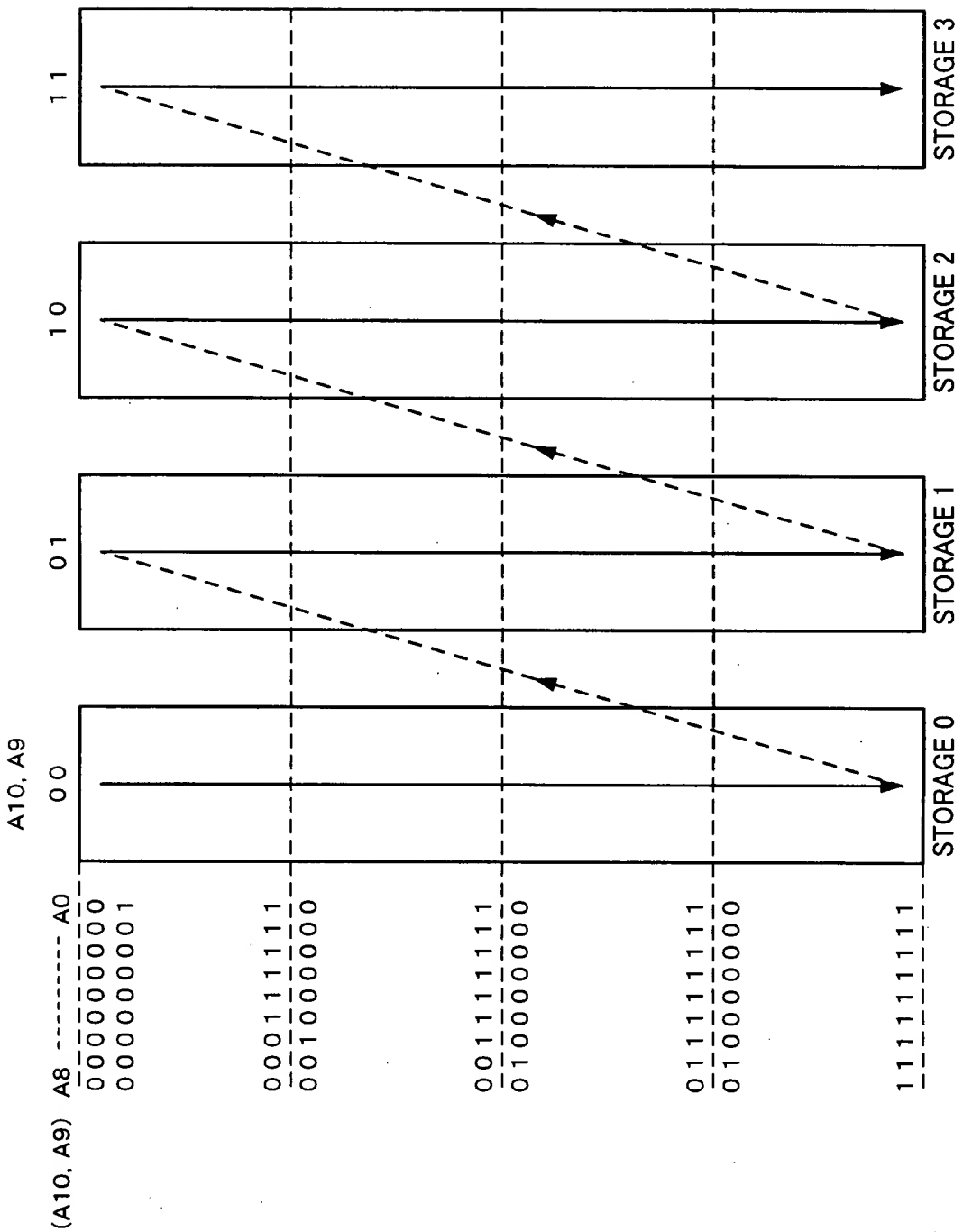
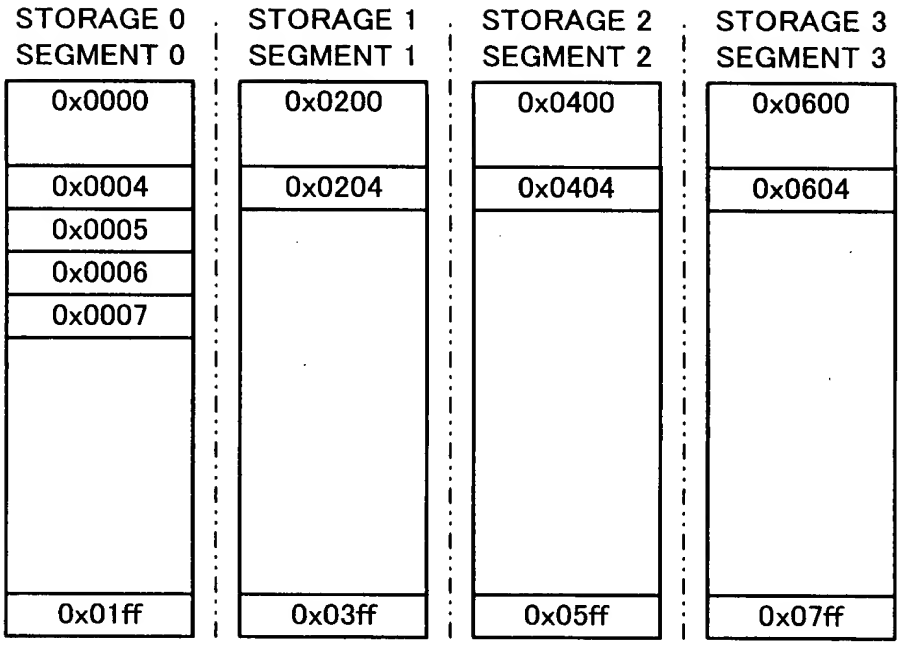

A10, A9
0 0
0 1
1 0
1 1
STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3
(A10, A9) A8 ---------- A0
0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 1
0 0 0 1 1 1 1 1 1
0 0 1 0 0 0 0 0 0
0 0 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0
0 1 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1 1

Fig. 21


STORAGE 0
SEGMENT 0
STORAGE 1
SEGMENT 1
STORAGE 2
SEGMENT 2
STORAGE 3
SEGMENT 3
0x0000
0x0004
0x0005
0x0006
0x0007
0x01ff
0x0200
0x0204
0x03ff
0x0400
0x0404
0x05ff
0x0600
0x0604
0x07ff

1.. CPU
5.. INTERFACE
6.. MEMORY CARD
7.. FLASH MEMORY